Numerical Study of Electronic Transport in Low-Dimensionality Materials for Future FETs

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The scaling of electronic devices has continued unabated for the past 5 decades, despite doomsday scenarios repeatedly predicting the "end of scaling". The "more than Moore" slogan has been, and still is, viewed by industry as a need to explore realistic low-to-medium-risk avenues, some already in production – such as strained Si/Ge or high-κ dielectrics, some yet to be translated to products in the near future or never – such III-V semiconductors or tunnel-FETs. On the contrary, Academia has looked (too?) far ahead, so much so that carbon-based electronics (carbon nanotubes, graphene, nanoribbons) is already considered *passée*. And now that the ULSI technology is looking at a feature size of 5 nm by 2026, even more "improbable" alternatives are considered, including transition metal dichalcogenides, silicene/ane, gernanene/ane (together with other *enes and *anes), topological insulators, Weyl semimetals, and other strongly correlated fermion systems.

Here we will first discuss the fact that, if we really wish to scale to 5 nm, simple electrostatic scaling laws demand that we take two-dimensional materials very seriously, despite the daunting practical difficulties we would face should we decide to "make them".[1] We will then consider whether graphene has any chance of replacing Si by looking at how the extremely promising electronic properties it exhibits in its ideal form become much less interesting when it becomes a component of some non-ideal structure (such when supported and gated and/or in nanoribbon form)[2]. Finally, we will discuss a couple of very interesting admittedly improbable but interesting ideas: 1. The Bose-Einstein condensation in bilayer systems (motivating UT-Austins BiSFETs) as an example of how issues of practical implementation may regrettably transform an excellent idea into a pure academic exercise[3]; and 2. Monolayer tin ("stannanane") as a 2D topological insulator with potential applications in spintronics and low-power high-performance devices (assuming that such layers can be fabricated)[4, 5]. For the entire discussion we will keep density functional theory (DFT), empirical pseudopotentials, and transport equations in the background.

Acknowledgments: Portions of this work have been performed in collaboration with Shela Aboud, Bo Fu, Jiseok Kim, Sudarshan Narayanan, Ana Suarez Negreira, Zhun-Yong Ong, and Cathy Sachs. The financial support of the Nanoelectronics Research Initiative (NRI/SRC) via a SWAN grant is thankfully acknowledged.

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