Numerical Simulation of Hetero Nanowire Tunnel Field Effect Transistors

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Tunnel Field Effect Transistors (TFETs) are candidates for low-power logic switches with steep (sub-thermal) slope which could enable a strongly reduced supply voltage. Device and circuit simulations of TFETs have shown a $8\times$ smaller delay-energy product at a supply voltage of 0.35 V compared to CMOS [1]. To improve the ON/OFF-current ratio, III-V/Si hetero junctions have been proposed [2]. Using nanowires has additional advantages: (i) the possibility of many different material combinations [3], (ii) efficient strain relaxation with shrinking diameter [3], (iii) a good electrostatic control due to the surrounding gate. Simulation results of this presentation are based on experimental data by Tomioka et al. [4,5,6] and Björk et al. [7] who advanced the integration of InAs nanowires on Si with nanometer-scale hetero epitaxy.

We show how the combined application of a quantum transport solver and a TCAD tool can help to understand the behavior of InAs/Si hetero nanowire Esaki diodes and TFETs leading to design guidelines for the optimization of geometry, doping, gating, and biasing. We used the massively parallel, multi-dimensional, and atomistic quantum transport simulator OMEN [8] which is based on a $sp^3d^5s^*$ tight-binding representation of the band structure. Quantum transport simulation can be done either in the Non-equilibrium Greens Function (NEGF) formalism, if electron-phonon scattering must be included, or using the much faster Wave Function formalism in the ballistic case. OMEN has been applied to direct and phonon-assisted band-to-band tunneling (BTBT) in InAs, Si, and Ge nanowire homo TFETs [9]. The commercial device simulator Sentaurus-Device [10] offers various local and non-local BTBT models. However, neither a theory nor an analytical model for BTBT in a hetero junction between a direct and an indirect semiconductor exist. A practical workaround has to be used with Sentaurus-Device, since a tunnel path across the hetero interface must either belong to a direct (zero-phonon) or to a phonon-assisted tunnel process. Therefore, the "*dynamic nonlocal path BTBT model*" [11], calibrated for InAs, is also used on the silicon side, fitted to experimental data of [12], whereas the calibrated model for Si [13] is also used on the InAs side after proper modifications.

First, the BTBT current of short, unconfined Esaki homo diodes ($\langle 111\rangle$, 20 nm length, abrupt doping) was simulated with OMEN for different materials and doping levels. For the direct materials (InAs, GaSb) and for Ge, where coherent BTBT is dominant [9], the simulation of bulk-like diodes is straightforward. Bulk simulations are needed because of the absence of geometrical confinement in the fabricated nanowire TFETs (diameters in the range 25 nm – 100 nm). It turns out that InAs has the highest BTBT current density, followed by GaSb and Ge. The upper limit for InAs is $\sim$ 10 MA/cm^2. In the case of Si, due to the demanding electron-phonon coupling, at least one-dimensional confinement has to be applied. The estimated bulk limit of Si remains below 100 kA/cm^2, a factor 500 smaller than that of InAs. The doping concentrations at the InAs side of InAs/Si nanowire hetero Esaki diodes produced at IBM Research-Zurich [14,15] are determined by reverse modeling. Measured InAs/Si nanowire TFET I_DV_{GS} characteristics [6] are then compared with calibrated TCAD simulations. Whereas the measured I_DV_{GS} curves show an almost constant slope over 2-3 orders of magnitude, a very weak ambipolarity, and a strong saturation of the ON-current for each source-drain voltage, simulation yields much higher ON-currents, a strong ambipolarity, curved slopes typical for BTBT, a minimum point slope of 45 mV/dec, and no ON-current saturation. The most likely explanation of the measured currents is that they are dominated by defect-assisted tunneling (DAT), either during interface or bulk Shockley-Read-Hall generation. Although multi-phonon coupling parameters of the involved defects in InAs are not known, the shape of the I_DV_{GS} curves can be qualitatively reproduced with a physics-based DAT model [16] in Sentaurus-Device. The apparent absence of BTBT in the measurement could be due to compressive biaxial strain in the highly lattice mismatched system.

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