Particle Detection with DEPFET Arrays in Gated Mode

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Arrays of Depleted Field effect Transistors (DEPFET) are mostly operated in rolling shutter mode. During this CCD like operation scheme one pixel row is read our while the others are collecting signals. For the very compact pixel design used for the Belle II pixel detector we found a very simple procedure to switch off the signal collection for the entire matrix preserving the information already stored in the pixel. In this way we are able to mask out the noise which may occur during and after bunch injection in the accelerator. The talk will cover the device related aspects of this new operation mode. 3D-device-simulations are used to gain an insight into the device and to optimize the pixel design. The feasibility of this very promising approach is demonstrated by laser and tests beam data taken on a Belle II test matrix.

The DEPFET (DEPleted Field Effect Transistor) is a semiconductor detector concept which combines detection and amplification within one device. A p-channel MOSFET is integrated onto a silicon detector substrate, which becomes fully depleted by a sufficiently high negative voltage applied to a p+ contact on the backside. A potential minimum is formed by sideward depletion, which is shifted directly underneath the transistor channel at a depth of about 1 µm by an additional phosphorus implantation underneath the external gate. Incident particles generate electron-hole pairs within the fully depleted bulk. While the holes drift into the back contact, electrons are accumulated in the potential minimum, called the internal Gate. If the transistor is switched on the electrons modulate the channel current. An amplification of more than 500pA per signal electron can be achieved with the technology currently available.
The removal of the signal charge and thermally generated electrons from the internal gate is called *Clear*. An n+ contact neighboring to the internal Gate is pulsed at a positive voltage providing a reach-through into the internal Gate. There is no any reset noise if the entire charge is completely removed. The probably most important feature of the DEPFET is the very small capacitance of the internal gate resulting in a low noise performance, even at room temperature and high operation speed. DEPFET arrays are usually operated in rolling shutter mode. Since only the addressed row is consuming power the rolling shutter mode is the most power efficient mode to operate a DEPFET array.
In an accelerator particle bunches have to be refreshed by additional injections. Since new bunches cannot be injected in the same phase space volume they have to cool by synchrotron radiation which leads to noisy bunches. Due to rolling shutter scheme any junk charge introduced by noisy bunches which hits the detector spoils the entire detector array. According to pessimistic estimations more than 20% of the data could be affected due to this phenomen at Belle II. Noisy bunches may appear every 10µs – the revolution time at Belle - in a well defined time window.
The pixel detector can be protected from noisy bunches if the DEPFET can be 'gated' into an insensitive (blind) mode during that time. Signals already collected in those pixel which were not yet readout have to be preserved during this blind phase. The basic idea of the 'gated mode' operation is to temporary provide an electrode which is much more attractive for electrons then the internal Gate. In the Belle DEPFET design the clear region is very large compared to Gate and the internal Gate beneath (see Fig. 1 and 2). The Figures illustrate the completely different charge collection behavior for Clear_hi =18V and Clear_low = 3V. During the noisy bunch phase the Clear lines of the entire matrix are raised at Clear_hi to protect the internal Gates from being hit. Related system aspects like high peak currents and cross talk are still under investigation.
The selectivity to the actual *Clear* process is given by the external Gate. During Clear the external Gate has to be switched to the on state (current is flowing). This provides the most possible negative potential of the internal Gateand the biggest potential difference between the Clear region and the internal Gate. Electrons can be emitted over the potential barrier inbetween. If the external Gate is switched off the hole channel at the surface disappears and the strong capacitive coupling between external and internal Gate leads to a much more positive potential in the latter one. Fig. 3 drafts the resulting potential slopes between internal Gate and Clear. Fig. 4. shows a measurement during blind mode. The removed charge is plotted versus the

external Gate voltage. The Clear suppression works very well.

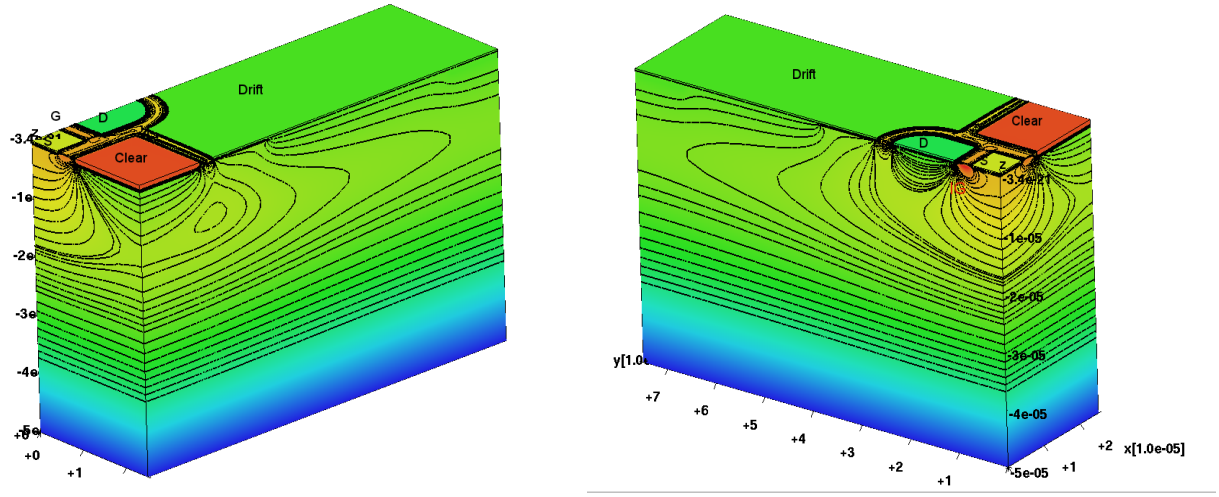

Fig. 1: 3D potential distributions of the 'collection state'. View on Clear and Drift regions (left) and on Drift, Drain (D), Source (S) and Gate (right). Clear is in off state (3V). Generated electrons drift into the internal Gate (IG). The simulation make use of Neumann boundary conditions. Every lateral boundary is a symmetric plane thus one half of a pixel is shown.

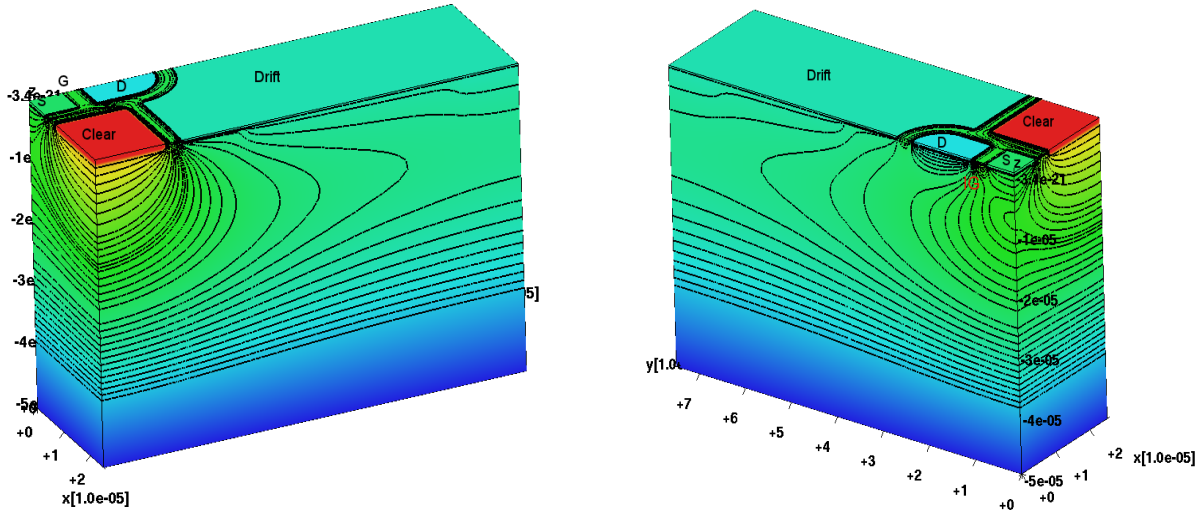

Fig. 2: 3D potential distributions of the 'blind state'. View on Clear and Drift regions (left) and on Drift, Drain (D), Source (S) and Gate (right). Clear is in on state (18V). Generated electrons drift into the Clear. The internal Gate (IG) is separated by potential barriers.

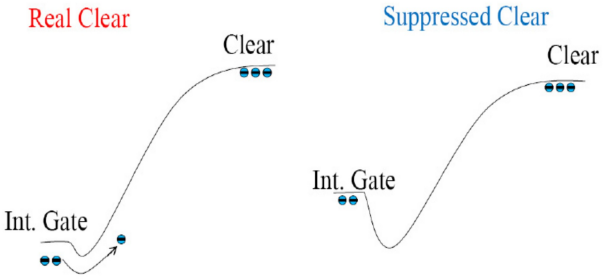

Fig. 3: Principle of the clear selectivity. Maximum potential between internal Gate and Clear during Real Clear and Suppressed Clear (blind mode)

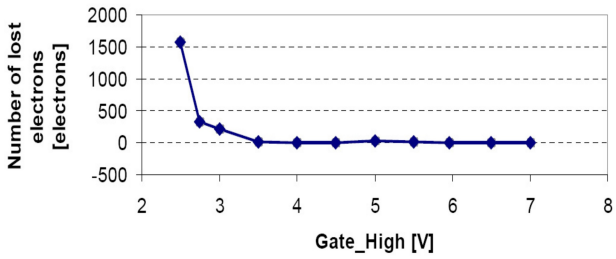

Fig. 4: Number of electrons removed from the internal Gate vs external Gate voltage. 12000 electrons were deposited before (laser illumination).