Physics and Modeling of Strain Effects in SiGe Heterojunction Bipolar Transistors

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Strain engineering is a key technological method for performance enhancement of state-of-the-art CMOS technologies. The effect of strain on the semiconductor band structure is exploited to manipulate carrier transport properties and device characteristics in a beneficial way. Strain plays also an essential role for the electrical behavior of SiGe heterojunction bipolar transistors (HBT). The SiGe base layer experiences a biaxial compression due to its lattice mismatch to the Si substrate. Since this stress is close to the stability limit of the SiGe layer reliability concerns have discouraged the use of further stress enhancement techniques in SiGe HBTs so far. Nevertheless, the device fabrication process imposes significant stresses in addition to the lattice mismatch stress which can have significant impact on device characteristics.

In this talk, we study the impact of process induced stress on the electrical characteristics of SiGe HBTs. Particularly large stresses are imposed by metal interconnects. We found experimentally that layout variations of aluminum metallization lines in the vicinity of a HBT can change collector currents by as much as 50% [1]. The main cause for this effect is uniaxial stress in the surface-normal direction imposed by the metal layer stack. The stress field and its effect on device characteristics can be calculated based on known mechanical properties and deformation potential theory.

Stress Simulation: The evolution of stress during the fabrication of a five-layer aluminum metallization was calculated taking into account the full thermal cycle of the process and measured intrinsic stress values of the individual layers. While the structured metal lines are essentially stress free at the deposition temperature (380°C) of the interlayer dielectrics they experience a strong tensile stress normal to the silicon surface when they are covered with oxide and cooled down to room temperature due to the large thermal expansion coefficient of aluminum. As a consequence, tensile stress up to 500 MPa is build up in transistor regions below a stack of 5 metal layers while adjacent Si regions without metal coverage are under compressive stress.

Device Simulation: Electrical characteristics of the strained HBTs were simulated within the drift-diffusion model. The effect of strain is taken into account by the splitting of electron and hole valleys according to deformation potential theory and k·p band structure. The mobility model includes modified inter-valley scattering due to strain splitting. The dominating effect of strain on the HBT characteristics is due to the strain dependence of the band gap in the SiGe base. Tensile strain in the surface-normal direction enhances the valley splitting introduced by lattice mismatch stress resulting in a reduced band gap in the base region of the HBT and in enhanced collector currents. The experimentally observed dependence of the collector current on the metal layout is well described by the presented simulation approach.

[1] H. Rücker, B.Heinemann, R. Barth, M. Lisker, IEEE IEDM Techn. Dig., pp. 34.5.1-4, 2011.